IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An article comprising: a storage medium having stored therein a memory array, said memory array comprising a programmable data element, and said storage medium also having stored therein instructions that when executed by a machine result in the following:

~~analyzing~~ providing data in a location of a memory array having a programmable data element, said location associated with a predetermined frame type of a received frame;

receiving an input signal indicating if said received frame contains an error; ~~and~~

providing an output signal indicating a negative receive response status if ~~said~~ an amount of count data is greater than a maximum frame length, and in response to said negative receive response checking the validity of said frame; ~~input signal indicates an error in said received frame.~~

checking a state of a first check bit and providing an output signal indicating a negative receive response status if said state of the first check bit indicates an unsupported state;

checking a state of a second check bit and providing an output signal indicating a positive reception status if the maximum frame length is not checked;

comparing the amount of count data for said received frame with the maximum frame length in said location of said memory associated with said predetermined frame type if the maximum frame length is to be checked; and

providing an output signal indicating a positive receive response status if said count data is less than or equal to said maximum frame length.

2. (Currently Amended) The article of claim 1, wherein said instructions that when executed by said machine also result in the following:

checking a state of a first check bit may include providing the first check bit of a row entry in the memory array associated with the predetermined frame type.

~~in said location of said memory array associated with said predetermined frame type, wherein a state of said first check bit indicates if said predetermined frame type is supported; and~~

~~providing said output signal indicating said negative receive response status if said state of said first check bit is in a first state.~~

3. (Previously Presented) The article of claim 2, wherein said programmable data element comprises said first check bit.

4. (Currently Amended) The article of claim 2, wherein said instructions that when executed by said machine also result in the following:

~~checking a state of a second check bit in said location of said memory array associated with said predetermined frame type;~~

~~comparing count data for said received frame with a frame length in said location of said memory associated with said predetermined frame type if said state of said second check bit is in a first state; and~~

~~providing said output signal indicating said negative receive response status if said count data is different than said frame length.~~

receiving a set-up frame before a subsequent data frame if the maximum frame length is variable.

5. (Previously Presented) The article of claim 4, wherein said programmable data element comprises said second check bit and said maximum frame length.

6. (Currently Amended) A system comprising:

a circuit card comprising an integrated circuit, said circuit card being capable of being coupled to a bus, said integrated circuit comprising a storage medium having stored therein a memory array, said memory array comprising a programmable data element, and said storage medium also having stored therein instructions that when executed by a machine result in the following:

~~analyzing~~ providing data in a location of a memory array having a programmable data element, said location associated with a predetermined frame type of a received frame;

receiving an input signal indicating if said received frame contains an error; ~~and~~

providing an output signal indicating a negative receive response status if ~~said~~ an amount of count data is greater than a maximum frame length, and in response to said negative receive response checking the validity of said frame; ~~input signal indicates an error in said received frame.~~

checking a state of a first check bit and providing an output signal indicating a negative receive response status if said state of the first check bit indicates an unsupported state;

checking a state of a second check bit and providing an output signal indicating a positive reception status if the maximum frame length is not checked;

comparing the amount of count data for said received frame with the maximum frame length in said location of said memory associated with said predetermined frame type if the maximum frame length is to be checked; and

providing an output signal indicating a positive receive response status if said count data is less than or equal to said maximum frame length.

7. (Currently Amended) The system of claim 6, wherein said instructions that when executed by said machine also result in the following:

checking a state of a first check bit in said location of said memory array associated with said predetermined frame type~~, wherein a state of said first check bit indicates if said predetermined frame type is supported; and~~

~~providing said output signal indicating said negative receive response status if said state of said first check bit is in a first state.~~

may include providing the first check bit of a row entry in the memory array associated with the predetermined frame type.

8. (Previously Presented) The system of claim 7, wherein said programmable data element comprises said first check bit.

9. (Currently Amended) The system of claim 7, wherein said instructions that when executed by said machine also result in the following:

~~checking a state of a second check bit in said location of said memory array associated with said predetermined frame type;~~

~~comparing count data for said received frame with a frame length in said location of said memory associated with said predetermined frame type if said state of said second check bit is in a first state; and~~

~~providing said output signal indicating said negative receive response status if said count data is different than said frame length.~~

receiving a set-up frame before a subsequent data frame if the maximum frame length is variable.

10. (Previously Presented) The system of claim 9, wherein said programmable data element comprises said second check bit and said frame length.

11. (Currently Amended) A method comprising:

~~receiving a frame;~~

~~determining a frame type of said frame;~~

~~accessing a location of memory associated with said frame type, said location comprising at least one programmable data element; and~~

~~checking a validity of said frame in response to data in said location of memory associated with said frame type.~~

providing data in a location of a memory array having a programmable data element, said location associated with a predetermined frame type of a received frame;

receiving an input signal indicating if said received frame contains an error;

providing an output signal indicating a negative receive response status if an amount of count data is greater than a maximum frame length, and in response to said negative receive response checking the validity of said frame;

checking a state of a first check bit and providing an output signal indicating a negative receive response status if said state of the first check bit indicates an unsupported state;

checking a state of a second check bit and providing an output signal indicating a positive reception status if the maximum frame length is not checked;

comparing the amount of count data for said received frame with the maximum frame length in said location of said memory associated with said predetermined frame type if the maximum frame length is to be checked; and

providing an output signal indicating a positive receive response status if said amount of count data is less than or equal to said maximum frame length.

12. (Currently Amended) The method of claim 11, wherein said programmable data element comprises a check bit indicating if said frame type is supported, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said check bit is in a first state.
the maximum frame length is variable.

13. (Currently Amended) The method of claim 11, further comprising:

~~counting data in said frame; and~~

~~comparing count data of said frame from said counting operation with a frame length in said location of memory associated with said frame type, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is different from said frame length.~~

receiving a set-up frame before a subsequent data frame if the maximum frame length is variable.

14. (Currently Amended) The method of claim 13, wherein ~~said frame length comprises a maximum frame length and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is greater than said maximum frame length.~~
said programmable data element comprises said first check bit.

15. (Previously Presented) The method of claim 11, further comprising:

receiving a first set up frame specifying a first frame type and a first frame length;

storing said first frame length in a location of memory associated with said first frame type;

receiving a second data frame immediately after said first set up frame; and

checking a validity of said second data frame in response to data in said location of memory associated with said first frame type from said first set up frame.

16. (Previously Presented) The method of claim 15, wherein said checking said validity of said second data frame comprises providing an output signal indicating a negative receive response status if a length of said second data frame is different than said first frame length.

17. (Previously Presented) The method of claim 15, wherein said first set up frame comprises a programmed input/output (PIO) Setup Frame Information Structure (FIS) and said second data frame comprises a data FIS.

18. (Currently Amended) An apparatus comprising:

~~circuitry capable of receiving a frame, determining a frame type of said frame, accessing a location of memory associated with said frame type, said location comprising at least one programmable data element; and~~

~~checking a validity of said frame in response to data in said location of memory associated with said frame type.~~

a received frame having a start of frame primitive, an end of frame primitive, a frame header and an FIS of a particular type;

a memory having an array including locations associated with a predetermined frame type;

a memory pointer circuit configured to interpret information from the received frame, the memory pointer circuit configured to point to a row entry in the array;

an error checking circuit configured to receive a CRC and the FIS from the frame, the error checking circuit configured to perform mathematical calculations and to provide an error calculation result signal to the memory;

a data count circuit configured to calculate a determined length of the FIS, the data count circuit configured to provide the determined length to the memory; and

a validation control circuit operatively connected with the memory, the validation control circuit configured to compare count data for the received frame with a maximum frame length in said location of said memory associated with said predetermined frame type if a maximum frame length is to be checked.

19. (Currently Amended) The apparatus of claim 18, ~~wherein said programmable data element comprises a check bit indicating if said frame type is supported, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said check bit is in a first state.~~

wherein the validation control circuit is configured to receive the error calculation result signal from the error checking circuit.

20. (Currently Amended) The apparatus of claim 18, wherein ~~said circuitry is further capable of counting data in said frame, and comparing count data of said frame from said counting operation with a frame length in said location of memory associated with said frame type, and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is different from said frame length.~~

the validation control circuit is configured to receive the determined length of the FIS from the data count circuit.

21. (Currently Amended) The apparatus of claim 20, wherein ~~said frame length comprises a maximum frame length and wherein said checking said validity of said frame comprises providing an output signal indicating a negative receive response status if said count data is greater than said maximum frame length.~~

the validation control circuit is configured to provide an output signal indicating a negative receive response status if said count data is greater than said maximum frame length, and in response to said negative receive response checking the validity of said frame.

22. (Currently Amended) The apparatus of claim ~~18~~ 21, wherein ~~said circuitry is further capable of receiving~~ the validation control circuit is configured to receive a first set up frame specifying a first frame type and a first frame length, storing said first frame length in a location of memory associated with said first frame type, receiving a second data frame immediately after said first set up frame; and

checking a validity of said second data frame in response to data in said location of memory associated with said first frame type from said first set up frame.

23. (Previously Presented) The apparatus of claim 22, wherein said checking said validity of said second data frame comprises providing an output signal indicating a negative receive response status if a length of said second data frame is different than said first frame length.

24. (Previously Presented) The apparatus of claim 22, wherein said first set up frame comprises a programmed input/output (PIO) Setup Frame Information Structure (FIS) and said second data frame comprises a data FIS.